THAT WHICH IS CLAIMED IS:

1. A method of fabricating a transistor, comprising:

forming a nitride-based channel layer on a substrate;

forming a barrier layer on the nitride-based channel layer;

forming a contact recess in the barrier layer to expose a contact region of the nitride-based channel layer;

forming a contact layer on the exposed contact region of the nitride-based channel layer using a low temperature deposition process;

forming an ohmic contact on the contact layer; and

forming a gate contact disposed on the barrier layer adjacent the ohmic contact.

2. The method of Claim 1, wherein the low temperature process uses a temperature of less than 960 °C.

3. The method of Claim 1, wherein the low temperature process uses a temperature of less than about 450 °C.

4. The method of Claim 1, wherein the low temperature process uses a temperature of less than about 200 °C.

5. The method of Claim 1, wherein the contact layer comprises an n-type degenerate semiconductor material other than GaN and AlGaN.

6. The method of Claim 5, wherein the contact layer comprises a non-nitride Group III-V semiconductor material, a Group IV semiconductor material and/or a group II-VI semiconductor material.

7. The method of Claim 1, wherein forming a contact layer on the exposed contact region of the nitride-based channel layer using a low temperature deposition process comprises forming a nitride-based contact layer by metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), plasma enchanced chemical vapor deposition (PECVD), sputtering and/or hydride vapor phase epitaxy (HVPE).

8. The method of Claim 1, wherein the low temperature deposition process is a process other than mass transport from a wafer on which the transistor is formed.

9. The method of Claim 1, further comprising:

forming a first dielectric layer on the barrier layer;

forming a gate recess in the first dielectric layer;

wherein forming a gate contact comprises forming a gate contact in the contact recess; and

wherein forming a contact recess comprises forming an ohmic contact recess in the first dielectric layer and the barrier layer that expose a portion of the nitride-based channel layer.

10. The method of Claim 9, wherein the first dielectric layer comprises a silicon nitride layer.

11. The method of Claim 10, wherein the silicon nitride layer provides a passivation layer for the transistor.

12. The method of Claim 1, further comprising:

forming a first dielectric layer on the barrier layer;

wherein forming a gate contact comprises forming a gate contact on the first dielectric layer; and

wherein forming a contact recess comprises forming an ohmic contact recess in the first dielectric layer and the barrier layer that expose a portion of the nitride-based channel layer.

13. The method of Claim 1, wherein the contact recess extends into the channel layer.

14. The method of Claim 1, wherein forming an ohmic contact comprises forming an ohmic contact without annealing the ohmic contact.

15. The method of Claim 1, wherein forming an ohmic contact comprises:
patterning a metal layer on the contact layer; and
annealing the patterned metal layer at a temperature of about 850 °C or less.

16. The method of Claim 1, wherein forming a contact layer on the exposed contact region of the nitride-based channel layer comprises forming a contact layer on the exposed contact region of the nitride-based channel layer to a thickness sufficient to provide a sheet resistivity of less than a sheet resistivity of a two-dimensional electron gas region formed at an interface between the channel layer and the barrier layer.

17. The method of Claim 1, wherein forming a contact layer comprises forming n-type InGaN, GaN, AlGaN, InAlGaN, InAlN and/or InN layer.

18. The method of Claim 17, wherein the InGaN, GaN, AlGaN, InAlGaN, InAlN and/or InN layer layer is doped with Si, Ge and/or O during formation.

19. The method of Claim 1, further comprising forming sidewalls of the channel layer to provide an increased surface area interface between the channel layer and the n-type contact layer as compared to a planar interface.

20. The method of Claim 19, wherein forming an ohmic contact on the n-type contact layer comprises forming an ohmic contact on the n-type contact layer that extends onto a portion of the channel layer.

21. The method of Claim 19, wherein forming an ohmic contact on the n-type contact layer comprises forming an ohmic contact on the n-type contact layer that terminates before the sidewall of the channel layer.

22. The method of Claim 1, further comprising:
forming holes in the channel layer adjacent the contact regions;
placing n-type nitride-based semiconductor material in the holes; and

wherein forming an ohmic contact on the n-type contact layer comprises forming an ohmic contact on the n-type contact layer and on the n-type nitride-based semiconductor material in the holes.

23. The method of Claim 1, wherein the contact recess comprises a first contact recess, the contact region comprises a first contact region and the ohmic contact comprises a first ohmic contact, the method further comprising:

forming a second contact recess in the barrier layer to expose a second contact region of the nitride-based channel layer;

forming a contact layer on the exposed second contact region of the nitride-based channel layer using a low temperature deposition process;

forming a second ohmic contact on the contact layer; and

wherein forming a gate contact comprises forming a gate contact disposed on the barrier layer between the first and second ohmic contacts.

24. The method of Claim 1, wherein forming a contact recess further comprises forming a contact recess that exposes a portion of the barrier layer and wherein forming a contact layer comprises forming a contact layer that extends onto the exposed portion of the barrier layer.

25. A method of fabricating a transistor, comprising:

forming a nitride-based channel layer on a substrate;

forming a barrier layer on the nitride-based channel layer;

forming a masking layer on the barrier layer;

patterning the masking layer and the barrier layer to provide a contact opening that exposes a portion of the nitride-based channel layer;

forming a contact layer on the exposed portion of the nitride-based channel layer and the masking layer;

selectively removing the masking layer and a portion of the contact layer on the masking layer to provide a nitride-based contact region;

forming an ohmic contact on the nitride-based contact region; and

forming a gate contact disposed on the barrier layer adjacent the ohmic contact.

26. The method of Claim 25, further comprising:

forming a first dielectric layer on the barrier layer;

forming a recess in the first dielectric layer;

wherein forming a gate contact comprises forming a gate contact in the recess;

wherein forming a masking layer on the barrier layer comprises forming a masking layer on the first dielectric layer; and

wherein patterning the masking layer and the barrier layer to provide a contact opening that exposes a portion of the nitride-based channel layer comprises patterning the masking layer, the first dielectric layer and the barrier layer to provide a contact opening that exposes a portion of the nitride-based channel layer.

27. The method of Claim 25, wherein the first dielectric layer comprises a silicon nitride layer.

28. The method of Claim 27, wherein the silicon nitride layer provides a passivation layer for the transistor.

29. The method of Claim 25, wherein the masking layer comprises a dielectric layer.

30. The method of Claim 29, wherein the dielectric layer comprises a silicon oxide layer.

31. The method of Claim 25, wherein the masking layer comprises a photoresist and/or e-beam resist masking layer.

32. The method of Claim 25, wherein forming an ohmic contact comprises forming an ohmic contact without annealing the ohmic contact.

33. The method of Claim 25, wherein forming an ohmic contact comprises:

patterning a metal layer on the nitride-based contact region; and

annealing the patterned metal layer at a temperature of less than about 850 °C.

34. The method of Claim 25, wherein forming a contact layer on the exposed portion of the nitride-based channel layer and the oxide layer comprises forming a nitride-based contact layer by metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), plasma enchanced chemical vapor deposition (PECVD), sputtering and/or hydride vapor phase epitaxy (HVPE).

35. The method of Claim 25, wherein forming a contact layer on the exposed portion of the nitride-based channel layer and the masking layer comprises forming a contact layer on the exposed portions of the nitride-based channel layer and the masking layer to a thickness sufficient to provide a sheet resistivity of less than a sheet resistivity of a two-dimensional electron gas region formed at an interface between the channel layer and the barrier layer.

36. The method of Claim 18, wherein forming a contact layer comprises forming n-type an InGaN, GaN, AlGaN, InAlGaN, InAlN and/or InN layer.

37. The method of Claim 29, wherein the InGaN, GaN, AlGaN, InAlGaN, InAlN and/or InN layer is doped with Si, Ge and/or O during formation.

38. The method of Claim 25, wherein the contact layer comprises an n-type degenerate semiconductor material other than GaN and AlGaN.

39. The method of Claim 38, wherein the contact layer comprises a non-nitride Group III-V semiconductor material, a Group IV semiconductor material and/or a group II-VI semiconductor material.

40. The method of Claim 25, further comprising forming sidewalls of the channel layer to provide an increased surface area interface between the channel layer and the contact layer in comparison to a planar interface.

41. The method of Claim 40, wherein forming an ohmic contact comprises forming an ohmic contact on the nitride-based contact region that extends onto a portion of the channel layer.

42. The method of Claim 40, wherein forming an ohmic contact comprises forming an ohmic contact on the nitride-based contact region that terminates before the sidewall of the channel layer.

43. The method of Claim 25, further comprising:

forming holes in the channel layer adjacent the contact regions;

wherein forming a contact layer further comprises placing a nitride-based semiconductor material in the holes; and

wherein forming an ohmic contact on the nitride-based contact region comprises forming an ohmic contact on the nitride-based contact regions and on the nitride-based semiconductor material in the holes.

44. The method of Claim 25, wherein the contact opening comprises a first contact opening, the nitride-based contact region comprises a first nitride-based contact region and the ohmic contact comprises a first ohmic contact, the method further comprising:

patterning the masking layer and the barrier layer to provide a second contact opening that exposes a portion of the nitride-based channel layer;

forming a contact layer on the portion of the nitride-based channel layer exposed by the second contact opening;

wherein selectively removing the masking layer comprises selectively removing the masking layer and a portion of the contact layer on the masking layer to provide the first nitride-based contact region and a second nitride-based contact region;

forming a second ohmic contact on the second nitride-based contact region; and

wherein forming a gate contact comprises forming a gate contact disposed on the barrier layer between the first and second ohmic contacts.

45. The method of Claim 25, wherein the contact recess exposes a portion of the barrier layer and wherein forming a contact layer comprises forming a contact layer that extends onto the exposed portion of the barrier layer.

46. A high electron mobility transistor, comprising:

a nitride-based channel layer on a substrate;

a barrier layer on the nitride-based channel layer;

at least one contact recess in the barrier layer that extends into the channel layer;

a contact region on the nitride-based channel layer in the contact recess;

a gate contact disposed on the barrier layer; and

wherein the contact region and the nitride-based channel layer include a surface area enlargement structure.

47. The transistor of Claim 46, wherein the surface area enlargement structure comprises patterned sidewalls of portions of the contact recess that extend into the channel layer.

48. The transistor of Claim 46, further comprising an ohmic contact on the contact region.

49. The transistor of Claim 48, wherein the ohmic contact does not extend onto the channel layer in the area of the sidewalls.

50. The transistor of Claim 48, wherein the ohmic contact extends onto the channel layer in the area of the sidewalls.

51. The transistor of Claim 48, wherein the surface area enlargement structure comprises holes extending into the channel layer having n-type semiconductor material therein and wherein the ohmic contact is in contact with the n-type nitride-based semiconductor material in the holes.

52. The transistor of Claim 46, wherein the contact region comprises InGaN, InAlGaN, InAlN and/or InN layer.

53. The transistor of Claim 46, wherein the contact region comprises AlGaN.

54. The transistor of Claim 46, wherein the contact region comprises GaN.

54. The transistor of Claim 46, wherein the contact region comprises InGaN, InAlGaN, InAlN, AlGaN, GaN and/or InN doped with Si, Ge and/or O.

55. The transistor of Claim 46, further comprising a silicon nitride layer on the barrier layer and wherein the gate contact is provided in a recess in the silicon nitride layer.

56. The transistor of Claim 48, wherein the ohmic contact comprises a first ohmic contact, the transistor further comprising a second ohmic contact adjacent the gate contact and opposite from the first ohmic contact.

57. The transistor of Claim 46, wherein the contact region comprises an n-type degenerate semiconductor material other than GaN and AlGaN.

58. The transistor of Claim 57, wherein the contact region comprises a non-nitride Group III-V semiconductor material, a Group IV semiconductor material and/or a group II-VI semiconductor material.

59. The transistor of Claim 46, wherein the contact region comprises a metal and/or metal alloy and provides an ohmic contact.

60. The transistor of Claim 46, wherein the contact region extends onto the barrier layer.

61. The transistor of Claim 46, further comprising a dielectric layer on the barrier layer and wherein the gate contact is on the dielectric layer.

62. A high electron mobility transistor, comprising:
a nitride-based channel layer on a substrate;
a barrier layer on the nitride-based channel layer;
contact recesses in the barrier layer that extend into the channel layer;
a contact region on the nitride-based channel layer in the contact recesses;
a gate contact disposed on the barrier layer; and

means for increasing a surface area of an interface between a vertical portion of the contact region and the nitride-based channel layer compared to a planar interface.

63. A method of fabricating a high electron mobility transistor, comprising:

forming a nitride-based channel layer on a substrate;

forming a barrier layer on the nitride-based channel layer;

forming at least one contact recess in the barrier layer that extends into the channel layer;

forming a contact region on the nitride-based channel layer in the contact recess;

forming a gate contact disposed on the barrier layer; and

wherein forming the contact region and forming the nitride-based channel layer include forming the contact region and forming the nitride-based channel layer to include a surface area enlargement structure.

64. The method of Claim 63, wherein forming the contact region and forming the nitride-based channel layer include forming the contact region and forming the nitride-based channel layer to include a surface area enlargement structure comprises patterning sidewalls of portions of the contact recess that extend into the channel layer.

65. The method of Claim 64, further comprising forming an ohmic contact on the nitride-based contact region.

66. The method of Claim 65, wherein forming an ohmic contact comprises forming an ohmic contact that does not extend onto the channel layer in the area of the sidewalls.

67. The method of Claim 65, wherein forming an ohmic contact comprises forming an ohmic contact that extends onto the channel layer in the area of the sidewalls.

68. The method of Claim 63, wherein forming the contact region and forming the nitride-based channel layer include forming the contact region and forming the nitride-based channel layer to include a surface area enlargement structure comprises:

forming holes extending into the channel layer;

placing n-type semiconductor material in the holes; and

forming an ohmic contact that is in contact with the n-type semiconductor material in the holes.

69. The method of Claim 63, wherein the contact region comprises InGaN, InAlGaN, InAlN and/or InN layer.

70. The method of Claim 63, wherein the contact region comprises AlGaN.

71. The method of Claim 63, wherein the contact region comprises GaN.

72. The method of Claim 63, wherein the contact region comprises InGaN, InAlGaN, InAlN, AlGaN, GaN and/or InN doped with Si, Ge and/or O.

73. The method of Claim 63, further comprising forming a silicon nitride layer on the barrier layer and wherein the gate contact is provided in a recess in the silicon nitride layer.

74. The method of Claim 63, wherein forming a contact region comprises forming a nitride-based semiconductor material contact region by metal organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), plasma enchanced chemical vapor deposition (PECVD), sputtering and/or hydride vapor phase epitaxy (HVPE).

75. The method of Claim 74. forming a contact region comprises forming an n-type semiconductor material contact region using a low temperature deposition process.

76. The method of Claim 63, further comprising:

forming a first ohmic contact on the contact region; and

forming a second ohmic contact adjacent the gate contact and opposite from the first ohmic contact.

77. The method of Claim 63, wherein the contact region comprises an n-type degenerate semiconductor material other than GaN and AlGaN.

78. The method of Claim 77, wherein the contact region comprises a non-nitride Group III-V semiconductor material, a Group IV semiconductor material and/or a group II-VI semiconductor material.

79. The method of Claim 63, wherein the contact region comprises a metal and/or metal allow to provide an ohmic contact.

80. The method of Claim 63, wherein the contact region extends onto the barrier layer.

81. A high electron mobility transistor, comprising:

a nitride-based channel layer on a substrate;

a barrier layer on the nitride-based channel layer;

at least one contact recess in the barrier layer that extends into the channel layer;

a region of metal and/or metal alloy on the nitride-based channel layer in the contact recess to provide an ohmic contact; and

a gate contact disposed on the barrier layer.

82. The transistor of Claim 81, wherein the region of metal extends onto the barrier layer.

83. A high electron mobility transistor, comprising:

a nitride-based channel layer on a substrate;

a barrier layer on the nitride-based channel layer;

at least one contact recess in the barrier layer that extends into the channel layer;

a region n-type degenerate semiconductor material other than GaN or AlGaN on the nitride-based channel layer in the contact recess;

an ohmic contact on the region of n-type degenerate semiconductor material; and

a gate contact disposed on the barrier layer.

84. The transistor of Claim 83, wherein the region of n-type degenerate semiconductor material extends onto the barrier layer.